

REMARKS

This amendment responds to the office action mailed July 15, 2004. In the office action the Examiner:

- objected to claims 3 and 13;
- objected to claims 11, 21-24 and 27-29 under 37 C.F.R. 1.75(c) as being of improper dependant form;
- rejected claims 1-6, 8, 10-16, 18, 19 and 21-29 under 35 U.S.C. 112, first paragraph;
- rejected claims 1-6, 8, 10-16, 18, 19 and 21-29 under 35 U.S.C. 112, second paragraph;
- rejected claims 1-6, 8, 10-16, 18, 19 and 21-29 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No. 6,738,943 (Jen) in view of Shimawaki et al (US 5,623,497).
- rejected claims 1-6, 8, 10-16, 18 and 19 under 35 U.S.C. § 103(a) as obvious over Satoh et al. (US 4,821,254) further considered with Ichikawa et al. (US 5,917,836) and both further considered with Shimawaki et al or LoGalbo et al. (US 6,128,763);
- rejected claims 21-29 under 35 U.S.C. § 103(a) as being unpatentable over the art as applied to claims 1, 8, 10 and 18, and further in view of Shimawaki et al. and Official notice.

After entry of this amendment, the pending claims are: claims 1-6, 8, 10-16, 18-19 and 21-29. Claims 7, 9, 17 and 20 were previously canceled.

Claim Objections

Applicant has amended claim 3 to recite that “the at least one error rate counter is reset periodically”. Support for claims 3 and 13 can be found in paragraph 0043 in connection with step 608 in Fig. 6 at which the error rate is “reset for every frame received from a compact disk”.

Claims 11 and 29, as amended, further define that the predetermined time period recited in the respective independent claims 10 and 18 corresponds to a time necessary to read a predetermined amount of data from the optical compact disk unit.

Claims 21-24 and 27-28 have been amended to conform with their respective parent apparatus claims 1, 8 and 18. Additionally, claims 22, 24 and 28 have been amended to recite the second remedial action that comprises (1) halting reading data from the optical disk media and (2) implementing a system optimization routine before reading data from the optical disk media. Support for the limitations found in these claims can be found, for

instance, in paragraph 0037 (see substitute specification, previously filed). For instance, paragraph 0037 identifies various system or device modifications that may be made during system optimization, by the system optimization routine. Furthermore, there are many references to system optimization throughout the specification, all of which make the term “system optimization routine” in the pending claims well defined for purposes of section 112, second paragraph.

Claim Rejections – 35 U.S.C. § 112

The Examiner has rejected claims 1-6, 8, 10-16, 18, 19 and 21-29 under **35 U.S.C. 112, first paragraph**. The Examiner contends that “the means/step of ‘demultiplexing a stream of error flag signals’ is ... not enabled by the disclosure”.

Applicant respectfully disagrees, because there is ample support in the specification for a demultiplexer that receives a stream of multiplexed error signals and outputs a stream of demultiplexed error signals (as recited in claims 1, 8 and 18, respectively) or a step for demultiplexing a stream of multiplexed error flag signals into a stream of demultiplexed error flag signals (as recited in claim 10). In Fig. 6, a stream of multiplexed encoded error data is received at step 602 and the stream of multiplexed data is then demultiplexed at step 604 to produce a number of demultiplexed bits of data (see also related disclosure in paragraph 0040). Moreover, Fig. 4 is actually a block diagram of a demultiplexer 402 that can be used in an embodiment of the present application in which a serially multiplexed stream of data is input into the demultiplexer 402 through bus 404 and the demultiplexed data is output in a parallel form.

The Examiner has also rejected claims 1, 3-7, 10-22, and 25-29 under 35 U.S.C. 112, first paragraph. The Examiner argues that the clock counter of claim 2 is critical or essential to the practice of the invention, but not included in claim 1. The Examiner also states that claim 1 with this additional limitation would be identical in scope to claim 8.

Applicant respectfully disagrees with the Examiner’s argument. First, the embodiment shown in Fig. 5 does not include the clock counter of claim 2. Furthermore, the Examiner attention is directed to paragraph 0045. Paragraph 0045 discusses Fig. 7, which includes counter 716, and explicitly discusses two embodiments, including an embodiment in which the clock counter is not used as stated in claim 2:

[0045] In an embodiment of the invention, a sector counter signal is sent on line 718 to C1 EPS count register 708 and C2 EPS count register 710 **upon every occurrence of a sector**

synchronization signal. In another embodiment, a sector count signal on line 718 is sent to C1 EPS count register 708 and C2 EPS count register 710 upon the occurrence of a predetermined number of sector synchronization signals on line 532. [emphasis added]

Stated differently, a clock counter operating as stated in claim 2 is not essential to the practice of the invention as defined by claims 1 and 18.

Second, claim 8 explicitly recites that the error type is derived from the Cross-Interleaved Reed-Solomon Code. In contrast, there is no such limitation to the error type in claim 1 or 18. Therefore, inclusion of a clock counter into claims 1 and 18 will not render them identical to claim 8.

The Examiner has also rejected claims 1-6, 8, 10-16, 18, 19 and 21-29 under **35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, Applicant has amended claims 1, 8 and 18 to recite a threshold rate register storing a predetermined threshold rate value.

In view of the discussion above, Applicant submits that the rejections under 35 U.S.C. 112, both first and second paragraph, should be withdrawn.

Double Patenting

The Examiner has rejected claims 1-6, 8, 10-16, 18-19 and 21-29 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No. 6738943 in view of Shimawaki.

Applicant encloses a terminal disclaimer, thereby addressing this rejection.

Claim Rejections – 35 U.S.C. § 103(a)

The Examiner has rejected claims 1-6, 8, 10-16, 18 and 19 under 35 U.S.C. 103(a) as obvious over Satoh further considered with Ichikawa and both further considered with Shimawaki or LoGalbo.

Claim 10 of the present invention is directed to a method of providing information on error rates occurring in an optical compact disk unit used for reading data from an optical disk media. The method first converts a stream of multiplexed error flag signals into a stream of demultiplexed error flag signals. The method then examines the demultiplexed error flag

signals for the occurrence of at least one error type over a predetermined time period, which is defined as an error rate for the error type. The method then compares the error rate with a predetermined threshold rate value and initiates different remedial actions in response to different comparison results.

For instance, if the error rate is nonzero, but does not exceed the predetermined threshold rate value, the method may respond by reducing the optical disk media's rotation speed so that there is more time available for reading a single data bit from the optical disk media. But if the error rate exceeds the predetermined threshold rate value, the method may respond by halting or altering predetermined operations within the optical compact disk unit.

However, none of cited references teach a method that initiates different remedial actions in response to different comparison results in order to reduce future data reading errors.

Satoh teaches a method of preventing errors caused by deterioration of a recording medium, e.g., an optical disk, from being detected during reproduction by identifying and marking those bad sectors if the number of errors in each of the bad sectors is greater than a predetermined number. It makes no claim or suggestion on how to reduce the number of errors by carefully initiating appropriate remedial actions under different conditions as recited in claim 10. For example, Satoh does not teach how to prevent data from being misread in the future based upon the data that has been read in the past.

Ichikawa teaches a method of reducing a capacity requirement for a memory by detecting data that is still being decoded, instead of waiting for the decoding of all the data to be completed. By doing so, the method offers more control over the decoding, as well as speedy access to the output of the decoded data. However, Ichikawa fails to disclose the limitation "comparing the at least one error rate to a predetermined threshold rate value". Nowhere in Ichikawa, including the disclosure from col. 9 line 40 to col. 12, line 50, suggests a parameter even close to the predetermined threshold rate value in claim 10. Furthermore, Ichikawa does not teach or suggest the limitation "initiating a first remedial action ... and a second remedial action ..." in order to reduce the probability of data misreading. As a matter of fact, the Examiner has never contended that Ichikawa teaches or suggests the comparing and initiating steps in the office action.

Shimawaki is directed to a bit error measurement apparatus that is capable of specifying bit error patterns in an incoming signal by measuring a bit error rate at a selected position or region of a test pattern that is used for verifying the incoming signal. In other

words, the apparatus attempts to reveal the true number of bit errors in the incoming signal without devoting any effort to correcting any of those errors through any remedial actions.

Finally, LoGalbo is directed to a transceiver device used for error correction in data networking in order to improve the network transmission efficiency. But both the Satoh and Ichikawa patents relate to data decoding and data reproduction from a disk, and the Shimawaki patent is in the field of bit error measurement of an incoming signal. In other words, the four cited references cover three distinct technical fields. As a result, there is a lack of motivation and reasonable expectation of success for one skilled in the art to combine the teachings of the four references to a method of reducing error rates when reading data from an optical compact disk medium.

Even more importantly, the combination of all four cited references, no matter how clever one skilled in the art may be, will not result in a method or apparatus that detects errors in data reproduced from an optical disk, and proactively changes system parameters in an effort to reduce the number of future errors.


In summary, claim 10 and its dependent claims 11-16 and 25-26 are patentable over the combined teachings of cited references, and furthermore combining the cited references as stated in the office action is improper because the only motivation for doing so is found in the present application.

Claims 1, 8 and 18 are three apparatus claims, each of which recites a comparator for comparing the average error rate with a predefined threshold rate value and initiating different remedial actions in accordance with different comparison results. Therefore, claims 1, 8 and 18 and their respective dependent claims 2-6, 21-22, 23-24, 19, 27-29 are also patentable over the cited references for at least the same reasons discussed above.

In light of the above amendments and remarks, Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-7501, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 14, 2004



Gary S. Williams

MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square, Suite 700
3000 El Camino Real
Palo Alto, California 94306
(650) 843-4000

31,066
(Reg. No.)